Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 10. A method of operating a flash memory device, wherein the flash memory device includes a P-type substrate, an N-type well region within the P-type substrate, a P-well region within the N-well region, a first memory cell and a second memory cell over the P-type substrate wherein the first memory cell has a first control gate and the second memory cell has a second control gate, a select gate between the first memory cell and the second memory cell, a first source/drain region and a second source/drain region in the P-well region on one side of the first memory cell and the second memory cell respectively, and the first source/drain region and the second source/drain region are N-type regions, the method comprising the steps of:
programming data into the first memory cell of the flash memory device includes:
applying a first positive voltage to the first control gate, applying a first negative voltage to the P-well region, connecting the select gate to ground and setting the first source/drain region and the second source/drain region in a floating state so that F-N tunneling effect is activated to program data into the first memory cell;

reading data from the first memory cell of the flash memory device includes:
applying a second positive voltage to the select gate, applying the second positive voltage to the first control gate, applying a third positive voltage to the second control gate, applying a fourth positive voltage to the second source/drain region and setting the first source/drain region and the P-well region in a floating state so that data can be read from the first memory cell; and
erasing data from the first memory device of the flash memory device, includes:
applying a fifth positive voltage to the select gate, setting the first control gate and the second control gate to 0V and setting the first source/drain region and the second source/drain region to a floating state so that F-N tunneling effect is activated to erase data from the flash memory device.

[c2] 11. The method of operating the flash memory device of claim 10, wherein the method may further include:
programming data into the second memory cell of the flash memory device, includes:
applying the first positive voltage to the second control gate, applying the first negative voltage to the P-well region, connecting the select gate to ground and setting the first source/drain region and the second source/

drain region to a floating state so that F-N tunneling effect is activated to program data into the second memory cell.

[c3] 12. The method of operating the flash memory device of claim 10, wherein data is also erased from the second memory cell when the data in the first memory data cell is erased.

[c4] 13. The method of operating the flash memory device of claim 10, wherein the first positive voltage is between about 10V to 12V.

[c5] 14. The method of operating the flash memory device of claim 10, wherein the first negative voltage is between about 6V to 8V.

[c6] 15. The method of operating the flash memory device of claim 10, wherein the second positive voltage is about 3.3V.

[c7] 16. The method of operating the flash memory device of claim 10, wherein the third positive voltage is about 10V.

[c8] 17. The method of operating the flash memory device of claim 10, wherein the fourth positive voltage is between about 1V to 1.5V.

[c9] 18. The method of operating the flash memory device of

claim 10, wherein the fifth positive voltage is between about 10V to 12V.